

Kent J. Tobin, Reg. No. 39,496, (650) 326-2400
Application No. 10/773,727; Atty. Docket No.: 021653-001500US
Title: Method and Structure of Manufacturing High Capacitance Metal on Insulator Capacitors in Copper
Applicant: Xian Jie Ning
Sheet 1 of 4 - REPLACEMENT SHEET

111 119 109 Barrier 121 105 101

Figure 1. To form a damascene structure build in IMD and metal Barrier is deposited. An array of VIAs are built for MIMCap

FIGURE 1

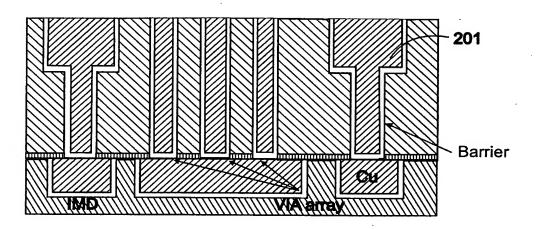


Figure 2. Cu seed, Plating and CMP are done the same way as Conventional dual-damascene Cu interconnect processes

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Sheet 2 of 4 - REPLACEMENT SHEET

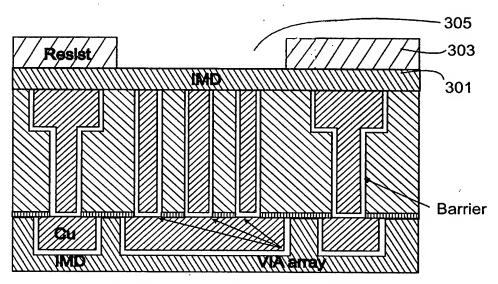


Figure 3. A layer of dielectric is deposited followed by a lithography Patterning to open the area where MIMCap need to be built.

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Title: Method and Structure of Manufacturing High Capacitance Metal on Insulator Capacitors in Copper
Applicant: Xian Jie Ning
Sheet 3 of 4 - REPLACEMENT SHEET

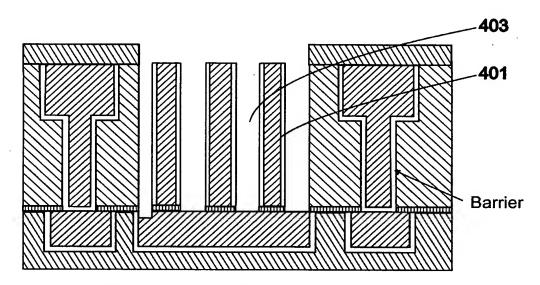


Figure 4. To selectively etch dielectric and strip the residual resist This process leaves Cu VIAs stand alone

FIGURE 4

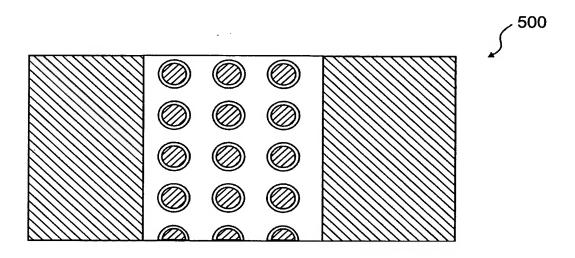


Figure 5. Top-view of Fig. 4.

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Sheet 4 of 4 - REPLACEMENT SHEET

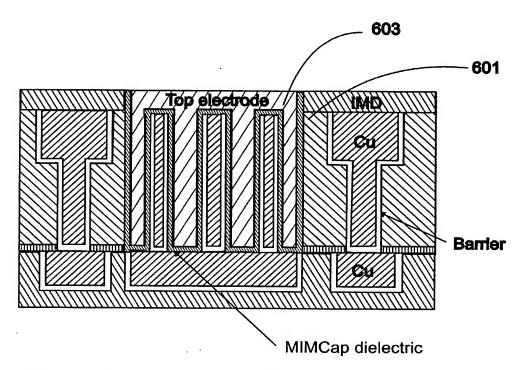


Figure 6. To conformaly deposit a MIMCap dielectric, a top metal electrode and CMP to have top electrode co-planar with IMD.